IN THE CLAIMS

1. (previously presented) A content addressable memory (CAM) system comprising:

a first CAM device having a priority number output, a first enable input, a CAM core to output a local match address, and a cascade logic circuit to output the local match address from the first CAM device in response to assertion of a first enable signal at the first enable input;

a second CAM device having a priority number input and an enable output coupled to the priority number output and the first enable input, respectively, of the first CAM device, the second CAM device further having a priority number output and an enable input; and

a third CAM device having a priority number input and an enable output coupled to the priority number output and the enable input, respectively, of the second CAM device.

2. (original) The system of claim 1 wherein the first CAM device additionally has a second enable input coupled to the enable output of the third CAM device.

3. (previously presented) The system of claim 1 further comprising an output bus coupled to each of the first, second and third CAM devices, and wherein the cascade logic circuit of the first CAM device is configured to output the match address onto the output bus in response to assertion of the first enable signal.

4. (previously presented) The system of claim 3 wherein the third CAM device comprises:

a CAM core to output a local match address and a local priority value in response to a compare instruction; and

a cascade logic circuit coupled to receive the local priority value from the CAM core and a remote priority value via the priority number input of the third CAM device, the cascade logic circuit being configured to assert a second enable signal via the enable output of the third CAM device if the remote priority value has a higher priority than the local priority value and to enable the local match address to be output onto the output bus if the local priority value has a higher priority than the remote priority value.

5. (previously presented) The system of claim 3 wherein the second CAM device comprises:

a CAM core to output a local match address and a local priority value in response to a compare instruction; and

a cascade logic circuit coupled to receive the local priority value from the CAM core and a remote priority value via the priority number input of the second CAM device, the cascade logic circuit being configured to assert the first enable signal via the enable output of the second CAM device if the remote priority value has a higher priority than the local priority value and to enable the local match address to be output onto the output bus if (1) the local priority value has a higher priority than the remote priority value and (2) if a second enable signal is received via the enable input of the second CAM device.

6. (previously presented) The system of claim 5 wherein the cascade logic circuit of the second CAM device is further configured to output the remote priority value via the priority number output of the second CAM device if the remote priority value has a higher priority than the local priority value and to output the local priority value via the priority number output of the second CAM device if the local priority value has a higher priority

than then remote priority value.

7. (previously presented) The system of claim 3 wherein the CAM core of the first CAM device comprises circuitry to output a local priority value that corresponds to the local match address and wherein the cascade logic circuit includes circuitry to receive the local priority value from the CAM core of the first CAM device and to output the local priority value via the priority number output of the first CAM device.

8. (previously presented) The system of claim 1 further comprising an output bus coupled to each of the first, second and third CAM devices, and wherein the first CAM device additionally has a second enable input coupled to the enable output of the third CAM device, and wherein the cascade logic circuit includes circuitry to output the local match address onto the output bus in response to assertion of the first enable signal if a second enable signal is received via the second enable input of the first CAM device.

9. (original) A content addressable memory (CAM) system comprising:
a first CAM device to output a first priority value;
a second CAM device coupled to receive the first priority value from the first CAM device and configured to output, as a winning priority value, a highest priority one of the first priority value and a second priority value; and
a third CAM device coupled to receive the winning priority value from the second CAM device and configured to output a first enable signal to the second CAM device if the winning priority value has a higher priority than a third priority value.

10. (original) The system of claim 9 further comprising an enable line coupled between the

second and third CAM devices to conduct the first enable signal from the third CAM device to the second CAM device, and wherein the enable line is additionally coupled to the first CAM device to conduct the first enable signal thereto.

11. (original) The system of claim 10 wherein the second CAM device is further configured to output a second enable signal to the first CAM device if the first priority value is the winning priority value.

12. (original) The system of claim 9 wherein the second CAM device is further configured to output a second enable signal to the first CAM device if (1) the first priority value is the winning priority value and (2) the first enable signal is output by the third CAM device.

13. (original) The system of claim 9 wherein the first CAM device includes a first CAM core to generate a first match address that corresponds to the first priority value, the second CAM device includes a second CAM core to generate a second match address that corresponds to the second priority value, and the third CAM device includes a third CAM core to generate a third match address that corresponds to the third priority value.

14. (original) The system of claim 13 wherein the third CAM device is further configured to output the third match address onto an output bus if the third priority value has a higher priority than the winning priority value.

15. (original) The system of claim 14 wherein the second CAM device is further configured to output the second match address onto the output bus if the third CAM device outputs the first enable signal and the second priority value is the winning priority value.

16. (original) The system of claim 15 wherein the first CAM device is coupled to receive the first enable signal from the third CAM device, and wherein the second CAM device is further configured to output a second enable signal to the first CAM device if the first priority value is the winning priority value, and wherein the first CAM device is further configured to output the third match address onto the output bus if (1) the first CAM device outputs the first enable signal and (2) the second CAM device outputs the second enable signal.

17. (original) The system of claim 14 wherein the second CAM device is further configured to output a second enable signal to the first CAM device if the third CAM device outputs the first enable signal and the first priority value is the winning priority value, and wherein the first CAM device is further configured to output the third match address onto the output bus in response to the second enable signal.

18. (previously presented) The system of claim 13 wherein each of the first, second and third CAM cores comprises a respective CAM array and a respective priority number storage circuit and is configured to:

compare a first comparand value with contents of the CAM array to identify one or more local priority values within the priority number storage circuit;

output a highest priority one of the one or more local priority values from the priority number storage circuit; and

generate a match address that identifies a storage location within the CAM array that corresponds to the highest priority one of the one or more local priority values.

19. (previously presented) The system of claim 18 wherein the highest priority one of the one or more local priority values output from the priority number storage circuit of the first CAM core constitutes the first priority value, the highest priority one of the one or more local priority values output from the priority number storage circuit of the second CAM core constitutes the second priority value, and the highest priority one of the one or more local priority values output from the priority number storage circuit of the third CAM core constitutes the third priority value.

20. (previously presented) The CAM device of claim 18 wherein each of the first, second and third CAM cores comprises match lines coupled between the CAM array and the priority number storage circuit, each match line corresponding to a respective row of CAM cells within the CAM array; and wherein each of the first, second and third CAM cores is further configured to generate match signals on the match lines according to whether contents of the corresponding rows of CAM cells match the comparand value, the match signals identifying the one or more local priority values.

21. (original) A content addressable memory (CAM) device comprising:

a CAM core to output a local priority number; and

a cascade logic circuit coupled to the CAM core to receive the local priority number and having an input to receive at least one remote priority number from another CAM device, the cascade logic circuit being configured to compare the local priority number and the at least one remote priority number at one of a plurality of different times according to a control value.

22. (original) The CAM device of claim 21 further comprising a configuration circuit coupled to the cascade logic to provide the control value thereto.

23. (original) The CAM device of claim 22 wherein the configuration circuit comprises a programmable non-volatile storage to store a configuration value, the configuration value including one or more bits that correspond to the control value.

24. (original) The CAM device of claim 22 wherein the configuration circuit is a one-time programmable circuit.

25. (previously presented) The CAM device of claim 22 wherein the CAM core comprises an instruction decoder being coupled to the configuration circuit and configured to store configuration information within the configuration circuit in response to a configuration instruction from a host device, the configuration information including one or more bits that correspond to the control value.

26. (previously presented) The CAM device of claim 25 wherein the configuration instruction includes information that indicates a disposition of the CAM device within a hierarchy of interconnected CAM devices.

27. (original) The CAM device of claim 26 wherein the instruction decoder is configured to store, within the configuration circuit, configuration information that indicates the one of the plurality of different times in accordance with the disposition of the CAM device within the hierarchy of interconnected CAM devices.

28. (original) The CAM device of claim 21 further comprising an interface to receive the control value.

29. (original) The CAM device of claim 28 wherein the interface comprises one or more integrated circuit contacts.

30. (original) A content addressable memory (CAM) device comprising:

a CAM core to generate a local priority value and corresponding match address; and

a cascade logic circuit coupled to receive the local priority value from the CAM core and having an input to receive a first enable signal from a first other CAM device, the cascade logic circuit being configured to compare the local priority value with a remote priority value received from a second other CAM device and to output a second enable signal to the second other CAM device if the remote priority value has a higher priority than the local priority value, the cascade logic circuit being further configured to enable the match address to be output from the CAM device if (1) the local priority value has a higher priority than the remote priority value and (2) the first enable signal is in a first state.

31. (original) The CAM device of claim 30 further comprising a configuration circuit coupled to the cascade logic circuit to provide a control value thereto, and wherein the cascade logic is further configured to compare the local priority value with the remote priority value at a time indicated by the control value.

32. (original) The CAM device of claim 31 further comprising an instruction decoder coupled to the configuration circuit and configured to store a configuration value therein in

response to a configuration instruction from a host device, the configuration value including one or more bits that correspond to the control value.

33. (original) The CAM device of claim 31 wherein the cascade logic circuit is further configured to disable the match address from being output from the CAM device if remote priority value has a higher priority than the local priority value or if the first enable signal is in a second state.

34. (original) The CAM device of claim 31 further comprising an output driver to output the match address from the CAM device if a control signal generated by the cascade logic circuit is in a drive-enable state, the cascade logic circuit being further configured to generate the control signal in the drive-enable state if (1) the local priority value has a higher priority than the remote priority value and (2) the first enable signal is in the first state.

35. (original) A method of operation within a first content addressable memory (CAM) device, the method comprising:

generating a local priority value and corresponding match address;

comparing the local priority value with a remote priority value received from a second CAM device;

outputting an enable signal to the second CAM device if the remote priority value has a higher priority than the local priority value; and

outputting the match address from the first CAM device if the local priority value has a higher priority than the remote priority value and an enable signal is received from a third CAM device.

36. (original) The method of claim 35 wherein outputting the match address comprises outputting the match address onto an output bus coupled to the first CAM device, second CAM device and third CAM device.

37. (original) The method of claim 35 wherein comparing the local priority value with the remote priority value comprises comparing the local priority value with the remote priority value at one of a plurality of different times indicated by a control value.

38. (original) The method of claim 37 further comprising storing the control value in a configuration circuit of the first CAM device.

39. (original) The method of claim 38 wherein storing the control value in the configuration circuit comprises storing the control value in the configuration circuit in response to a command from a host device.

40. (original) A method of operation within a content addressable memory (CAM) system, the method comprising:

outputting a first priority value from a first CAM device;

comparing a second priority value with the first priority value within a second CAM device and outputting a highest priority one of the first and second priority values; and

comparing a third priority value with the highest priority one of the first and second priority values within a third CAM device and, if the highest priority one of the first and second priority values has a higher priority than the third priority value, outputting a first enable signal from the third CAM device to the second CAM device.

41. (original) The method of claim 40 further comprising outputting a second enable signal from the second CAM device to the first CAM device if the first value has a higher priority than the second value.

42. (original) The method of claim 41 wherein outputting the second enable signal from the second CAM device to the first CAM device comprises outputting the second enable signal from the second CAM device to the first CAM device if (1) the first value has a higher priority than the second value and (2) the first enable signal is output from the third CAM device to the second CAM device.

43. (original) The method of claim 41 further comprising:

generating a match address within the first CAM device, the match address corresponding to the first priority value; and

outputting the match address onto a result bus coupled to the first, second and third CAM devices if the second enable signal is output from the second CAM device to the first CAM device.

44. (original) The method of claim 41 wherein outputting the first enable signal from the third CAM device to the second CAM device comprises outputting the first enable signal from the third CAM device to the first and second CAM devices.

45. (original) The method of claim 44 further comprising:

generating a match address within the first CAM device, the match address corresponding to the first priority value; and

outputting the match address onto a result bus coupled to the first, second and third CAM

devices if (1) the second enable signal is output from the second CAM device to the first CAM device and (2) the first enable signal is output from the third CAM device to the first CAM device.

46. (original) The method of claim 40 further comprising:

generating a match address within the second CAM device, the match address corresponding to the second priority value; and

outputting the match address onto a result bus coupled to the first, second and third CAM devices if (1) the first enable signal is output from the third CAM device to the second CAM device and (2) the second priority value has a higher priority than the first priority value.

47. (original) The method of claim 40 further comprising:

generating a match address within the third CAM device, the match address corresponding to the third priority value; and

outputting the match address onto a result bus coupled to the first, second and third CAM devices if the third priority value has a higher priority than the highest priority one of the first and second priority values.

48. (original) The method of claim 40 wherein each of first, second and third priority values comprises a respective N-bit value, N being an integer greater than one.

49. (original) The method of claim 40 wherein outputting a highest priority one of the first and second priority values comprises outputting a numerically lowest one of the first and second priority values.

50. (original) A content addressable memory (CAM) device comprising:

means for generating a local priority value and corresponding match address;

means for comparing the local priority value with a remote priority value received from a first other CAM device;

means for outputting an enable signal to the first other CAM device if the remote priority value has a higher priority than the local priority value; and

means for outputting the match address to an external signal path if the local priority value has a higher priority than the remote priority value and an enable signal is received from a second other CAM device